

CLAIMS:

1. A method of forming memory circuitry comprising a memory array having a plurality of memory capacitors and comprising peripheral memory circuitry operatively configured to write to and read from the memory array, comprising:

forming a dielectric well forming layer over a semiconductor substrate;

removing a portion of the well forming layer effective to form at least one well within the well forming layer;

forming an array of memory cell capacitors within the well; and

forming the peripheral memory circuitry laterally outward of the well forming layer memory array well.

2. The method of claim 1 wherein the well forming layer consists essentially of doped silicon dioxide.

3. The method of claim 1 wherein the well has a well base which is substantially planar.

4. The method of claim 1 wherein the semiconductor substrate comprises word lines having insulative caps and the well has a well base, the removing leaving a lowest portion of the well base at least 2000 Angstroms above the caps.

1 5. The method of claim 1 wherein the capacitors respectively
2 comprise a portion which has a container shape.

3
4 6. The method of claim 1 wherein the capacitors respectively
5 comprise a portion which has a container shape, the portion being
6 formed to be partially received within the well forming layer beneath
7 the well.

8
9 7. A method of forming memory circuitry comprising a memory
10 array having a plurality of memory capacitors and comprising peripheral
11 memory circuitry operatively configured to write to and read from the
12 memory array, comprising:

13 forming a dielectric well forming layer over a semiconductor
14 substrate;

15 removing a portion of the well forming layer effective to form at
16 least one well within the well forming layer, the well having a well
17 base;

18 forming an array of capacitor storage node openings through the
19 well base into the well forming layer over storage node contact
20 locations;

21 supporting an array of storage node capacitor electrodes within the
22 well and base openings therein by the well forming layer; and

23 forming the peripheral memory circuitry laterally outward of the
24 well forming layer memory array well.

1 8. The method of claim 7 wherein the well base is
2 substantially planar.

3
4 9. The method of claim 7 wherein the semiconductor substrate
5 comprises word lines having insulative caps, the removing leaving a
6 lowest portion of the well base at least 2000 Angstroms above the caps.

7
8 10. The method of claim 7 wherein the capacitors respectively
9 comprise a portion which has a container shape, the portion being
10 formed to be partially received within the well forming layer beneath
11 the well base.

11. A method of forming memory circuitry comprising a memory array having a plurality of memory capacitors and comprising peripheral memory circuitry operatively configured to write to and read from the memory array, comprising:

forming a dielectric well forming layer over a semiconductor substrate;

removing a portion of the well forming layer effective to form at least one well within the well forming layer;

forming a capacitor storage node forming layer within the well;

forming an array of capacitor storage node openings within the capacitor storage node forming layer within the well;

forming capacitor storage node electrode within the capacitor storage node forming layer openings;

after forming the capacitor storage node electrodes, removing at least some of the capacitor storage node forming layer from within the well; and

forming the peripheral memory circuitry laterally outward of the well.

1 12. The method of claim 11 comprising forming an etch stop
2 layer within the well prior to forming the capacitor storage node
3 forming layer, the removing of at least some of the capacitor storage
4 node forming layer comprising etching using a chemistry which is
5 substantially selective to remove the capacitor storage node forming layer
6 relative to the etch stop layer.

7
8 13. The method of claim 11 wherein the well is substantially
9 planar.

10
11 14. The method of claim 11 wherein the semiconductor substrate
12 comprises word lines having insulative caps and the well has a well
13 base, the removing leaving a lowest portion of the well base at least
14 2000 Angstroms above the caps.

15
16 15. The method of claim 11 wherein the capacitors respectively
17 comprise a portion which has a container shape, the portion being
18 formed to be partially received within the well forming layer beneath
19 the well.

20
21 16. The method of claim 11 comprising removing substantially
22 all of the capacitor storage node forming layer from within the well
23 after forming the capacitor storage node electrodes.

1 17. The method of claim 11 wherein,
2 the capacitors respectively comprise a portion which has a
3 container shape, the portion being formed to be partially received within
4 the well forming layer beneath the well; and
5 removing substantially all of the capacitor storage node forming
6 layer from within the well after forming the capacitor storage node
7 electrodes.

1 18. A method of forming dynamic random access memory
2 circuitry comprising:

3 forming an array of word lines over a semiconductive substrate;
4 forming a substantially planar dielectric well forming layer over the
5 word lines;

6 etching at least one well into the well forming layer which defines
7 a dynamic random access memory array area within the well and
8 dynamic random access peripheral circuitry area laterally outward of
9 well, the well having a substantially planar base;

10 depositing a dielectric etch stop layer over the well forming layer
11 laterally outward of and to within the well to less than completely fill
12 the well;

13 forming a dielectric storage node forming layer over the etch stop
14 layer laterally outward of and to within the well to overfill the well;

15 etching an array of capacitor storage node openings within the
16 well through the storage node forming layer, through the etch stop layer
17 and into the well forming layer over storage node contact locations;

18 depositing a capacitor storage node layer over the storage node
19 forming layer to within the capacitor storage node openings to less than
20 completely fill the capacitor storage node openings;

21 removing the capacitor storage node layer from outwardly of the
22 storage node forming layer effective to form capacitor storage node
23 containers within the capacitor storage node openings in electrical
24 connection with the storage node contact locations, the capacitor storage

1 node containers having top surfaces received elevationally proximate an
2 outermost surface of the dielectric etch stop layer;

3 after forming the capacitor storage node containers, etching the
4 capacitor storage node forming layer using the dielectric etch stop layer
5 as an etch stop and exposing lateral outer container surface area of the
6 capacitor containers;

7 forming a capacitor dielectric layer and a cell electrode layer over
8 the capacitor storage node containers including the outer container
9 surface area of the capacitor containers; and

10 forming the dynamic random access peripheral memory circuitry
11 laterally outward of the well.

12
13 19. The method of claim 18 comprising forming the capacitor
14 storage node containers to have the top surfaces received elevationally
15 above the outermost surface of the dielectric etch stop layer by less
16 than 50 Angstroms.

17
18 20. The method of claim 18 wherein the dielectric storage node
19 forming layer is initially formed to be non-planar, and further
20 comprising planarizing the dielectric storage node forming layer prior to
21 etching the array of capacitor storage node openings.

1 21. The method of claim 18 comprising etching substantially all
2 of the capacitor storage node forming layer from the substrate after
3 forming the capacitor storage node electrodes and before forming the
4 capacitor dielectric layer.

1 22. A method of forming dynamic random access memory
2 circuitry comprising:

3 forming an array of word lines over a semiconductive substrate;

4 forming an array of digit lines over the word lines;

5 forming a substantially planar dielectric well forming layer over the
6 word lines and digit lines;

7 etching at least one well into the well forming layer which defines
8 a dynamic random access memory array area within the well and
9 dynamic random access peripheral circuitry area laterally outward of
10 well, the well having a substantially planar base;

11 depositing a dielectric etch stop layer over the well forming layer
12 laterally outward of and to within the well to less than completely fill
13 the well;

14 forming a dielectric storage node forming layer over the etch stop
15 layer laterally outward of and to within the well to overfill the well;

16 planarizing the storage node forming layer while effectively leaving
17 the etch stop layer covered by the storage node forming layer;

18 etching an array of capacitor storage node openings within the
19 well through the storage node forming layer, through the etch stop layer
20 and into the well forming layer over storage node contact locations;

21 depositing a capacitor storage node layer over the storage node
22 forming layer to within the capacitor storage node openings to less than
23 completely fill the capacitor storage node openings;

1 removing the capacitor storage node layer from outwardly of the
2 storage node forming layer effective to form capacitor storage node
3 containers within the capacitor storage node openings in electrical
4 connection with the storage node contact locations, the capacitor storage
5 node containers having top surfaces received elevationally proximate an
6 outermost surface of the dielectric etch stop layer;

7 after forming the capacitor storage node containers, etching
8 substantially all of the capacitor storage node forming layer from the
9 substrate using the dielectric etch stop layer as an etch stop and
10 exposing lateral outer container surface area of the capacitor containers;

11 forming a capacitor dielectric layer and a cell electrode layer over
12 the capacitor storage node containers including the outer container
13 surface area of the capacitor containers; and

14 forming the dynamic random access peripheral memory circuitry
15 laterally outward of the well.

16
17 23. The method of claim 22 wherein the well forming layer
18 consists essentially of doped silicon dioxide.

19
20 24. The method of claim 22 wherein the well etching leaves the
21 well base at least 1000 Angstroms above outermost tops of the digit
22 lines.

1 25. The method of claim 22 comprising forming the capacitor
2 storage node containers to have the top surfaces received elevationally
3 above the outermost surface of the dielectric etch stop layer by less
4 than 50 Angstroms.

5
6 26. Memory circuitry comprising:

7 a semiconductor substrate;

8 a plurality of word lines received over the semiconductor
9 substrate;

10 an insulative layer received over the word lines and the substrate,
11 the insulative layer having at least one well formed therein, the well
12 comprising a base received over the word lines, the well peripherally
13 defining an outline of a memory array area, area peripheral to the well
14 comprising memory peripheral circuitry area;

15 a plurality of memory cell storage capacitors received within the
16 well over the word lines; and

17 peripheral circuitry within the peripheral circuitry area operatively
18 configured to write to and read from the memory array.

19
20 27. The memory circuitry of claim 26 wherein the base is
21 substantially planar.

1 28. The memory circuitry of claim 26 wherein the word lines
2 have insulative caps and the well base has a lowest portion which is
3 received at least 2000 Angstroms above the caps.

4
5 29. The memory circuitry of claim 26 comprising buried digit
6 lines, the well base having a lowest portion which is received at least
7 1000 Angstroms above outermost tops of the digit lines.

8
9 30. The memory circuitry of claim 26 comprising buried digit
10 lines and wherein the base is substantially planar, and the well base
11 being received at least 1000 Angstroms above outermost tops of the
12 digit lines.

13
14 31. The memory circuitry of claim 26 wherein the insulative
15 layer has a substantially planar outermost surface, and the capacitors
16 have capacitor storage node electrodes having topmost surfaces received
17 elevationally proximate the substantially planar outermost surface of the
18 insulative layer.

19
20 32. The memory circuitry of claim 26 wherein the insulative
21 layer is formed to have a substantially planar outermost surface, and
22 the capacitors have capacitor storage node electrodes having topmost
23 surfaces received elevationally above the substantially planar outermost
24 surface of the insulative layer by less than 50 Angstroms.

33. Memory circuitry comprising:

a semiconductor substrate;

an insulative layer received over the substrate, the insulative layer having at least one well formed therein, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the well, the memory cell storage capacitors respectively comprising a storage node container which is received partially within the insulative layer through the well base; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

34. The memory circuitry of claim 33 wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Angstroms above the caps.

35. The memory circuitry of claim 33 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

1 36. The memory circuitry of claim 33 wherein the insulative
2 layer has a substantially planar outermost surface, and the capacitors
3 have capacitor storage node electrodes having topmost surfaces received
4 elevationally proximate the substantially planar outermost surface of the
5 insulative layer.

6
7 37. The memory circuitry of claim 33 wherein the insulative
8 layer is formed to have a substantially planar outermost surface, and
9 the capacitors have capacitor storage node electrodes having topmost
10 surfaces received elevationally above the substantially planar outermost
11 surface of the insulative layer by less than 50 Angstroms.

1 38. Dynamic random access memory circuitry comprising:
2 a semiconductor substrate;
3 word lines received over the semiconductor substrate;
4 an insulative layer received over the word lines and the substrate,
5 the insulative layer having at least one well formed therein, the well
6 comprising a base received over the word lines, the well peripherally
7 defining an outline of a memory array area, area peripheral to the well
8 comprising memory peripheral circuitry area, the well having a
9 substantially planar base;
10 a plurality of memory cell storage capacitors received within the
11 well, the memory cell storage capacitors respectively comprising a
12 storage node container which is received partially within the insulative
13 layer through the well base over the word lines; and
14 peripheral circuitry within the peripheral circuitry area operatively
15 configured to write to and read from the memory array.

16
17 39. The memory circuitry of claim 38 wherein the insulative
18 layer has a substantially planar outermost surface, and the capacitors
19 have capacitor storage node electrodes having topmost surfaces received
20 elevationally proximate the substantially planar outermost surface of the
21 insulative layer.
22
23
24

1 40. The memory circuitry of claim 38 wherein the insulative
2 layer is formed to have a substantially planar outermost surface, and
3 the capacitors have capacitor storage node electrodes having topmost
4 surfaces received elevationally above the substantially planar outermost
5 surface of the insulative layer by less than 50 Angstroms.

6
7 41. The memory circuitry of claim 38 comprising buried digit
8 lines, the well base having a lowest portion which is received at least
9 1000 Angstroms above outermost tops of the digit lines.

10
11 42. Dynamic random access memory circuitry comprising:
12 a semiconductor substrate;
13 word lines received over the semiconductor substrate;
14 bit lines received over the word lines;
15 an insulative layer received over the word lines, the digit lines
16 and the substrate, the insulative layer having at least one well formed
17 therein, the well comprising a base received over the word lines and
18 the digit lines, the well peripherally defining an outline of a memory
19 array area, area peripheral to the well comprising memory peripheral
20 circuitry area;

21 a plurality of memory cell storage capacitors received within the
22 well over the word lines and the digit lines; and

23 peripheral circuitry within the peripheral circuitry area operatively
24 configured to write to and read from the memory array.

1 43. The memory circuitry of claim 42 wherein the insulative
2 layer has a substantially planar outermost surface, and the capacitors
3 have capacitor storage node electrodes having topmost surfaces received
4 elevationally proximate the substantially planar outermost surface of the
5 insulative layer.

6
7 44. The memory circuitry of claim 42 wherein the insulative
8 layer is formed to have a substantially planar outermost surface, and
9 the capacitors have capacitor storage node electrodes having topmost
10 surfaces received elevationally above the substantially planar outermost
11 surface of the insulative layer by less than 50 Angstroms.

1 45. Dynamic random access memory circuitry comprising:
2 a semiconductor substrate;
3 word lines received over the semiconductor substrate;
4 bit lines received over the word lines;
5 an insulative layer received over the word lines, the digit lines
6 and the substrate, the insulative layer having at least one well formed
7 therein, the well comprising a substantially planar base received over the
8 word lines and the digit lines, the well peripherally defining an outline
9 of a memory array area, area peripheral to the well comprising memory
10 peripheral circuitry area;
11 a plurality of memory cell storage capacitors received within the
12 well, the memory cell storage capacitors respectively comprising a
13 storage node container which is partially received within the insulative
14 layer through the well base; and
15 peripheral circuitry within the peripheral circuitry area operatively
16 configured to write to and read from the memory array.

17
18 46. The memory circuitry of claim 45 wherein the insulative
19 layer has a substantially planar outermost surface, and the capacitors
20 have capacitor storage node electrodes having topmost surfaces received
21 elevationally proximate the substantially planar outermost surface of the
22 insulative layer.

1 47. The memory circuitry of claim 45 wherein the insulative
2 layer is formed to have a substantially planar outermost surface, and
3 the capacitors have capacitor storage node electrodes having topmost
4 surfaces received elevationally above the substantially planar outermost
5 surface of the insulative layer by less than 50 Angstroms.